Impact of Buffer Architecture on the Performance of Heterogeneously Integrated III-V-on-Si Solar Cells

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***Abstract* — We have demonstrated the impact of buffer architectures on the performance of 1J GaAs solar cells heterogeneously integrated on Si. An all-epitaxial molecular beam epitaxy-grown thin (<1 µm) hybrid GaAs/Ge "virtual" buffer approach provided 1J GaAs cell efficiency of ~10% on Si, as compared with cell structures with thick 3 µm GaAs buffers. Solar cell results were further corroborated with materials analysis to provide a clear path for the reduction of performance-limiting dislocations. The thin "Ge-on-Si" virtual buffer approach to III-V-on-Si cell structures in the current work indicates a promising future for monolithically integrated, low-cost and high-efficiency III-V-on-Si photovoltaics.**

***Index Terms* – III-V Semiconductor materials, III-V on Si, Photovoltaic cells, Silicon, Germanium.**

I. Introduction

The global energy landscape is projected to change remarkably in the coming decades with dwindling carbon based resource reserves and escalating energy demands. The looming energy crisis coupled with climate change concerns will necessitate large scale adoption of cleaner alternatives, such as solar energy. However, for widespread commercial and domestic adoption of photovoltaics, the levelized cost of solar generated electricity must become competitive with sources such as oil or coal. Achieving high efficiency solar cells and driving down cell costs have been key objectives for PV researchers in order to become more self-sufficient in the energy sector. In this pursuit, while the performance of silicon (Si)-based solar cells have almost saturated at an efficiency of 25.6%, III-V compound semiconductor-based solar cells have steadily outperformed all other PV technologies, with a record efficiency of 46% (~29% for 1J) **[1]** thus far. Si is the undisputed standard in the PV industry; thus, to make a significant step forward in the pursuit of high efficiency solar cells, a promising approach will be to integrate the superior properties of compound semiconductors with the mature technology of Si. Successful monolithic integration of high efficiency III-V cells with low cost, abundant Si substrates will enable the unification of the performance merits of III-V cells with the cost benefits and superior mechanical and thermal properties of Si.

The fundamental challenges of GaAs on Si epitaxy lie in the 4% lattice mismatch between GaAs and Si, the growth of a polar compound semiconductor on non-polar Si, and the large difference (63%) in thermal coefficient between GaAs and Si, thereby leaving the photoactive region sensitive to dislocations, anti-phase boundaries and cracking **[2]**.

In this work, we investigate the performance of single junction (1J) GaAs cells grown on Si using *two different all-epitaxial III-V/IV buffer approaches* as an alternative to current III-V cells grown on expensive and smaller diameter germanium (Ge) or GaAs substrates. The initial approach is the direct epitaxy of GaAs cells on Si using a thick GaAs buffer and understanding the required base thickness to compensate for dislocations propagating into the active region. The second approach is to introduce a thin Ge epilayer between the Si substrate and GaAs buffer, thereby creating a virtual "Ge-on-Si" template for subsequent GaAs growth. This approach decouples two challenges, *viz*. that of lattice mismatched growth and polar on non-polar epitaxy, at separate interfaces. Moreover, the Ge-on-Si template can be further extended to develop a hybrid Ge-Si active junction below the GaAs cell, where the Ge layer serves as the emitter in a bottom Si sub-cell. The aim of this work is to elucidate the role of the Ge epilayer and to enable thinner III-V-on-Si solar cell structures, reducing manufacturing cost while preserving the electrical performances of these devices.

II. Experiment

Fig. 1 shows the different cell structures studied in this work, of which Sample A and Sample B use a 2 µm GaAs buffer grown directly on Si, whereas Sample C is comprised of a 144

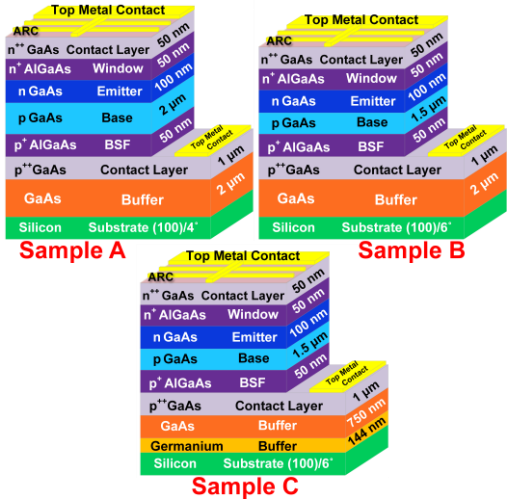

Fig. 1. Schematic diagrams of the solar cell structures with different buffer architectures studied in this work.

nm Ge intermediate layer with a 750 nm GaAs buffer on top. All structures were grown on Si substrates offcut 4-6° towards the <110> direction, thus creating a double stepped interface for anti-phase domain (APD) free GaAs growth on non-polar Si (Ge), in a dual chamber molecular beam epitaxy system. Migration enhanced epitaxy (MEE) was used to nucleate GaAs in Samples A and C but not in Sample B, where only low temperature GaAs nucleation was performed. In Sample C, a two-step LT/HT growth process enabled two-dimensional growth at low temperatures, forming a template for subsequent smooth, high quality Ge layer growth at high temperature with fewer threading dislocations. Growth temperatures were varied from a minimum of 400°C for GaAs nucleation up to 530°C at the surface. Multiple annealing steps were included in each buffer growth to annihilate dislocations propagating into the active cell region, which adversely affect the cell performance.

The active 1J *n*-on-*p* GaAs cell in Sample A has a 2 µm base, in comparison to a 1.5 µm base region in Sample B and Sample C. Be and Si were used for the *p* and *n*-type dopant sources across all samples. The $Al_xGa_{1-x}As$ composition was modified from $Al_{0.25}Ga_{0.75}As$ in the back surface reflection layer to $Al_{0.71}Ga_{0.29}As$ in the window layer to accommodate a large bandgap window with reduced broad-spectrum absorption. Growth temperature was closely monitored in the back surface reflector (BSR) and window layer to mitigate the effect of difference in Ga and Al ad-atom mobilities. After completion of each growth, the samples were gradually cooled down to prevent any thermal cracking prior to unloading for characterization and fabrication.

III. MATERIAL CHARACTERIZATION

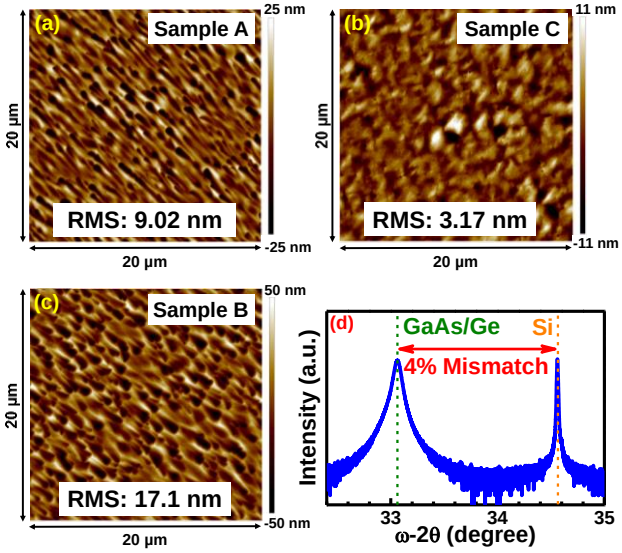

Fig. 2. (a-c) AFM micrographs indicating surface roughness of GaAs top contact layer for each sample, respectively, and (d) (004) X-ray rocking curve of Sample C to show the metamorphic nature of the composite GaAs/Ge buffer.

The use of Al in the BSR and window layer increases surface roughness, and hence surface recombination velocity (SRV) of minority carriers in the 1J active cell, due to the low ad-atom mobility of Al and its subsequent clustering. The use of an offcut substrate further increases susceptibility of the cell surface to roughness. The surface roughness of the top GaAs contact layer of each sample was studied. As shown in the AFM micrographs in Fig. 2, for a scan size of 20×20 μm^2 the RMS roughness measured was 9.02 nm for Sample A, 17.1 nm for Sample B and 3.17 nm for Sample C. This suggests that, despite the lower thermal budget given to atoms during surface reconstruction in Sample C and a 6˚ offcut substrate, the low temperature Ge nucleation and MEE assisted GaAs nucleation on Ge preserves a significantly smoother surface through the cell growth. On the contrary, Sample B suffers from high surface roughness, which can be contributed to the absence of MEE during GaAs nucleation on offcut Si. Comparing Samples A and C, it was found that the Ge intermediate layer reduces surface roughness, which would result in a lower SRV in the III-V cell. Moreover, the X-ray rocking curve from Sample C, seen in Fig. 2(d), shows a fully relaxed GaAs/Ge peak alongside the Si substrate peak, indicating successful Ge-on-Si epitaxy and enabling a virtual Ge template for the subsequent GaAs buffer.

Cross-sectional TEM micrographs of Samples A, B and C, shown in Fig. 3, revealed APD-free growth, thus indicating that substrate offcut suppressed the initiation of inversion domain boundaries at the III-V/IV interface. The low resolution X-TEM images of the entire device stack show low propagation of misfit induced defects into the active device beyond the GaAs buffer layer. Despite its significantly reduced thickness, the hybrid III-V/IV buffer in Sample C can be seen to effectively minimize threading dislocations from the lattice

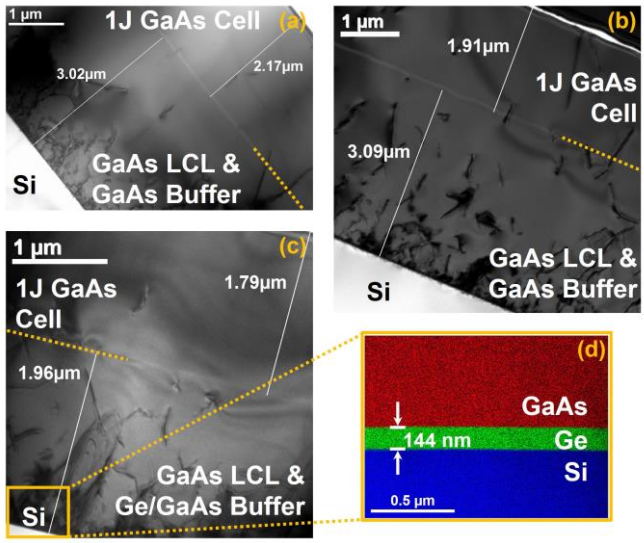

Fig. 3. (a-c) Low magnification TEM micrographs of each sample, respectively, and (d) EDS elemental map of the composite GaAs/Ge buffer layer interfaces in Sample C.

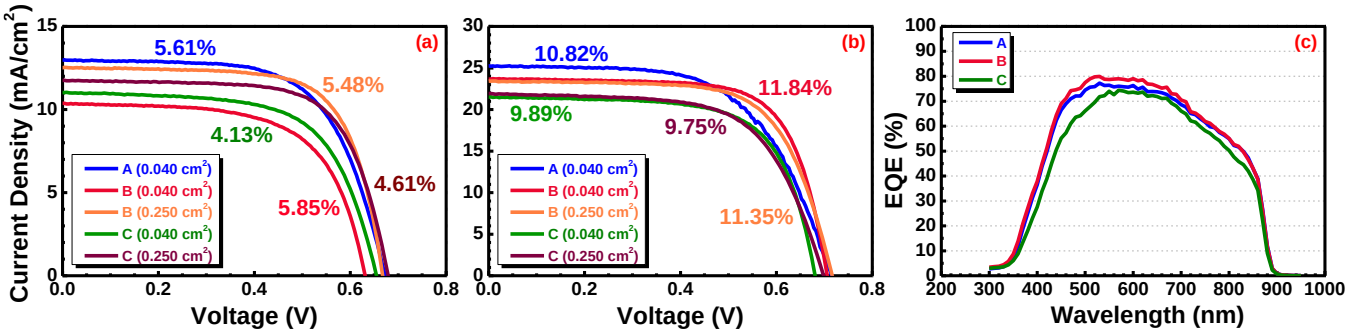

Fig. 4. I-V characteristics with cell efficiency indicated of Samples A, B and C (a) before etching out the top contact layer, (b) after etch and ARC deposition of the same, (c) external quantum efficiency (EQE) response of samples with incident light spectra.

mismatched Si-Ge heterointerface.

Energy-dispersive X-ray spectroscopy (EDS) elemental mapping helps corroborate the GaAs/Ge buffer quality on Si. Fig. 3(d) shows a three-element overlay of Ge, Si, and As, where the red corresponds to As content, blue corresponds to Ge content, and green corresponds to Si content. Three distinct, uniform color regions corresponding to GaAs (red), Ge (blue) and Si (green) layers are clearly visible with no evidence of interdiffusion at the interfaces, which would have been indicated by a mixing of colors in the EDS map. Several dislocations that migrate into the buffer can be seen to annihilate, likely caused by thermal annealing during growth. Furthermore, no micro-twins or stacking faults were observed, demonstrating good crystal quality across samples.

IV. ELECTRICAL PERFORMANCE

Solar cells have been fabricated on Samples A, B and C with front metal contacts and a bilayer anti-reflection coating (ARC) deposited on the exposed cell area. To better understand the effect of defects in the active region, cells of dimensions (0.5 cm × 0.5 cm) and (0.2 cm × 0.2 cm) were processed on Samples B and C. Figs. 4(a), (b) depict the I-V characteristics of fabricated cells at both pre-cap etch and post ARC deposition stages, and Table 1 enlists critical performance parameters for the latter. The short circuit current density is observed to increase by 100% after etching and ARC deposition due to a lack of contact-layer photon adsorption and minimized reflection from the cell surface. Cell performance is still limited by dislocations threading into the base region, as can be observed from the external quantum efficiency graph in Fig. 4(c), which shows a flat spectral response for higher energy photons between 475 nm to 675 nm, but drops steadily for higher wavelengths. Smaller area (0.040 cm^2) cells, expected to be less sensitive to defects, corroborate with slightly higher efficiencies. Overall, there is high uniformity between output parameters of cells of both sizes. Sample A suffers from high series resistance losses that limit its fill factor, likely stemming from a reduced lifetime of minority carriers in its thicker base, as the fabrication process is consistent across all cells. Sample C, with a 900 nm buffer as opposed to a 2 µm buffer in Samples A and B, gives competent results; inferring that the 144 nm Ge intermediate layer enables a very thin buffer layer in this promising approach to designing high efficiency GaAs cells on Si.

TABLE 1
OUTPUT PERFORMANCE PARAMETERS FOR DIFFERENT CELL SIZES ON EACH SAMPLE AFTER ARC DEPOSITION

Sample #	Cell Area (cm^2)	V_{oc} (V)	J_{sc} (mA/cm^2)	Fill Factor (%)	Efficiency η (%)
Sample A	0.040	0.715	25.232	59.98	10.82
Sample B	0.040	0.705	23.684	70.86	11.84
Sample B	0.25	0.716	23.42	67.7	11.35
Sample C	0.040	0.68	21.493	67.6	9.887
Sample C	0.25	0.698	21.88	63.83	9.75

V. CONCLUSION

We have demonstrated a novel design for the monolithic integration of III-V solar cells on Si utilizing an intermediate Ge layer, which can serve both as a buffer layer or an active layer to realize a hybrid Ge-Si bottom sub-cell. Introduction of this group IV epilayer facilitates a thin buffer system to mitigate mismatch induced defects within the buffer layer and reduce their effect on conversion efficiency of subsequent active junctions. Furthermore, our approach utilizing the MEE of polar III-V semiconductors on offcut Si substrates resolves two fundamental challenges of surface roughness and inverse domain boundary formation in these solar cells. This virtual "Ge-on-Si" template, when optimized to minimize threading dislocations from the lattice mismatched interface, indicates a promising future for monolithically integrated, low-cost and high-efficiency III-V-on-Si photovoltaics.

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